FIG.1

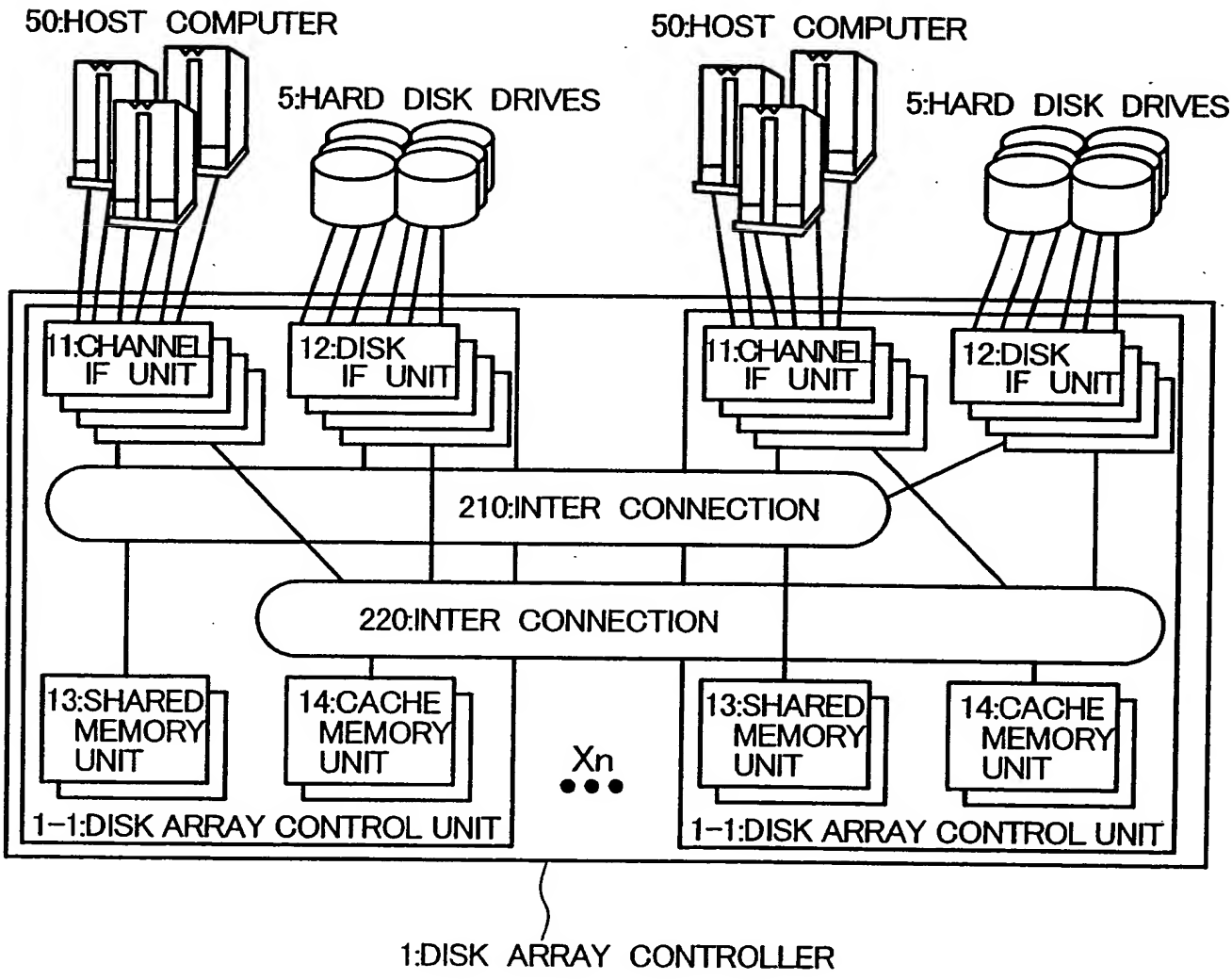
50:HOST COMPUTER
5:HARD DISK DRIVES
50:HOST COMPUTER
5:HARD DISK DRIVES
11:CHANNEL IF UNIT
12:DISK IF UNIT
11:CHANNEL IF UNIT
12:DISK IF UNIT
210:INTER CONNECTION
220:INTER CONNECTION
13:SHARED MEMORY UNIT
14:CACHE MEMORY UNIT
Xn
13:SHARED MEMORY UNIT
14:CACHE MEMORY UNIT
1-1:DISK ARRAY CONTROL UNIT
1-1:DISK ARRAY CONTROL UNIT
1:DISK ARRAY CONTROLLER

FIG.2
(PRIOR ART)

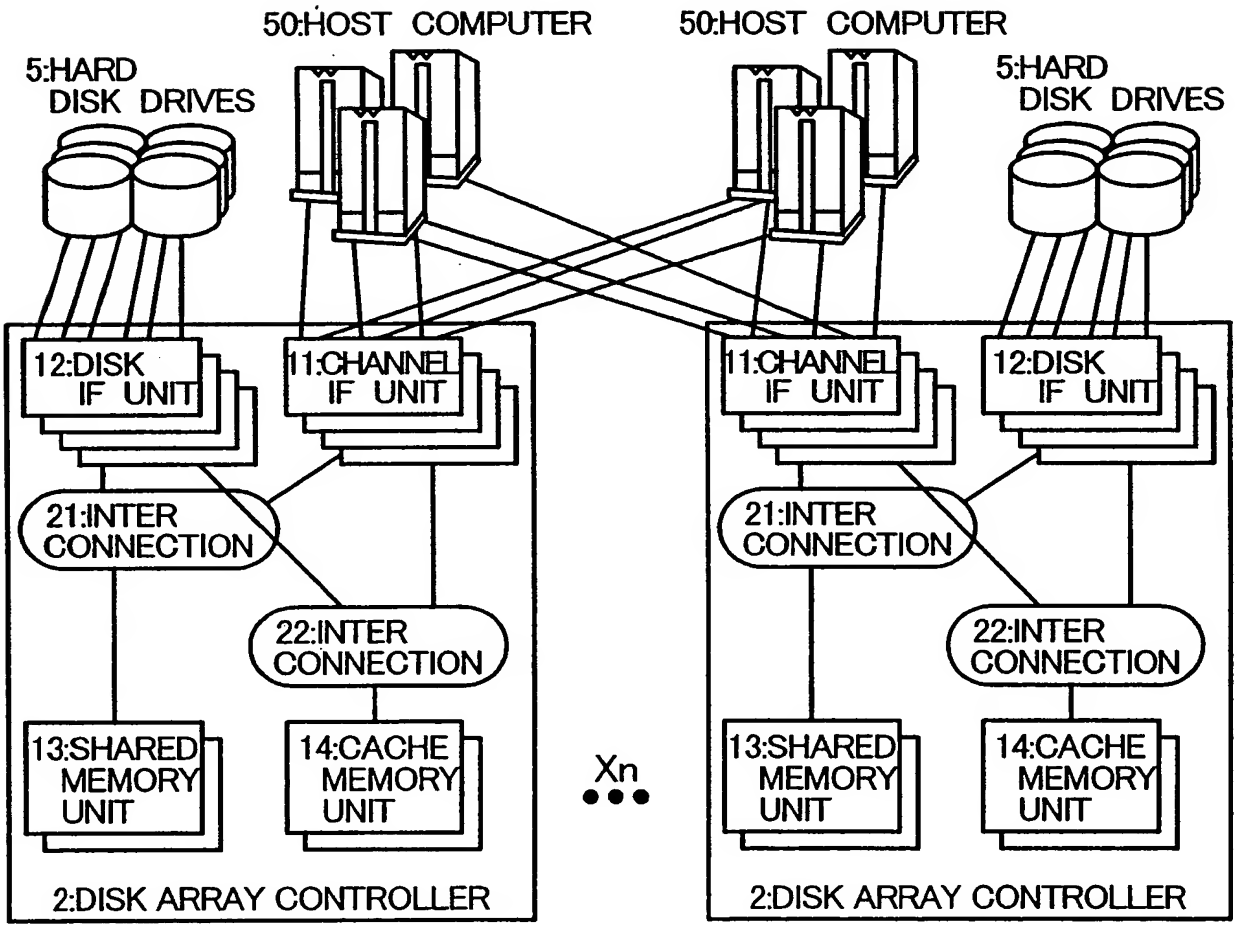

FIG.3
(PRIOR ART)

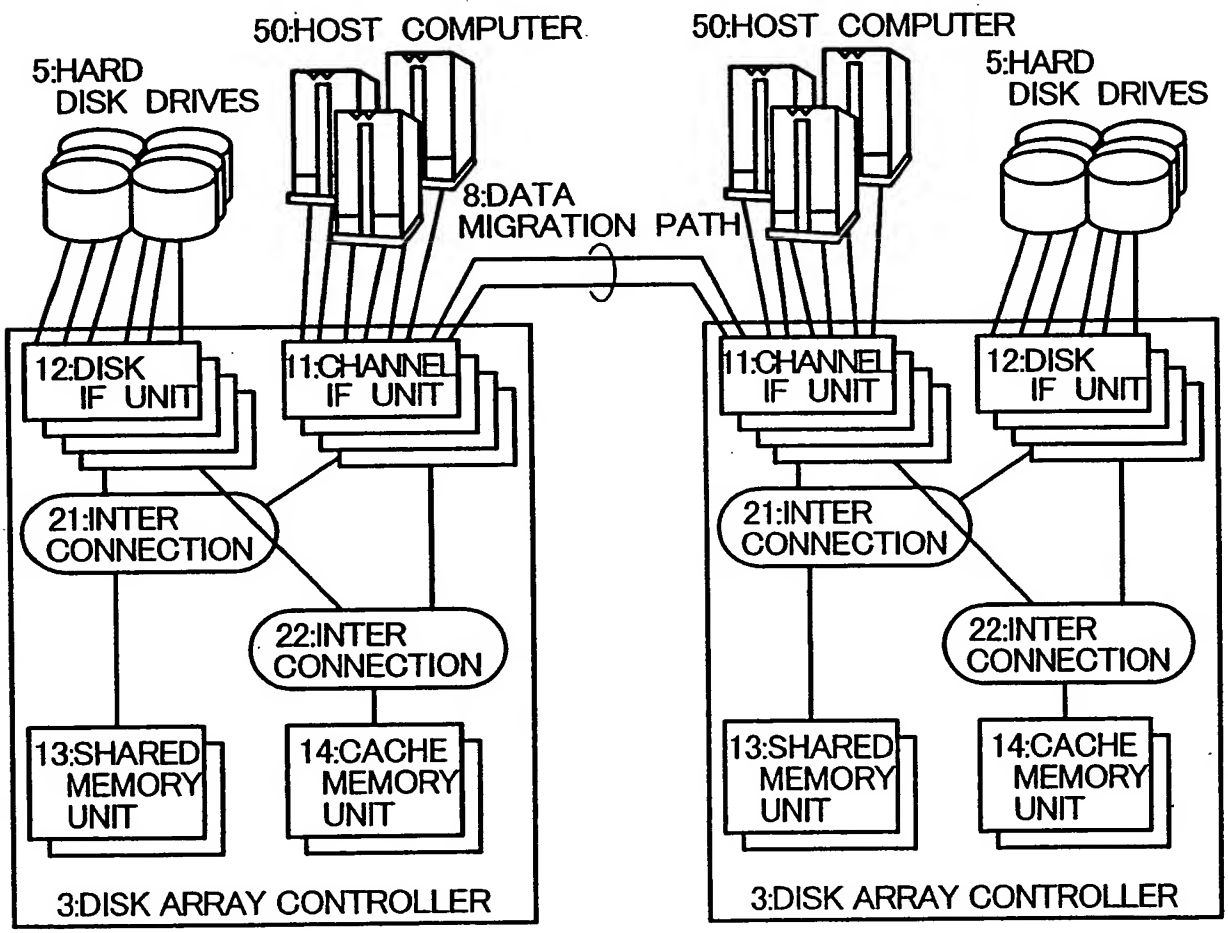

FIG.4
(PRIOR ART)

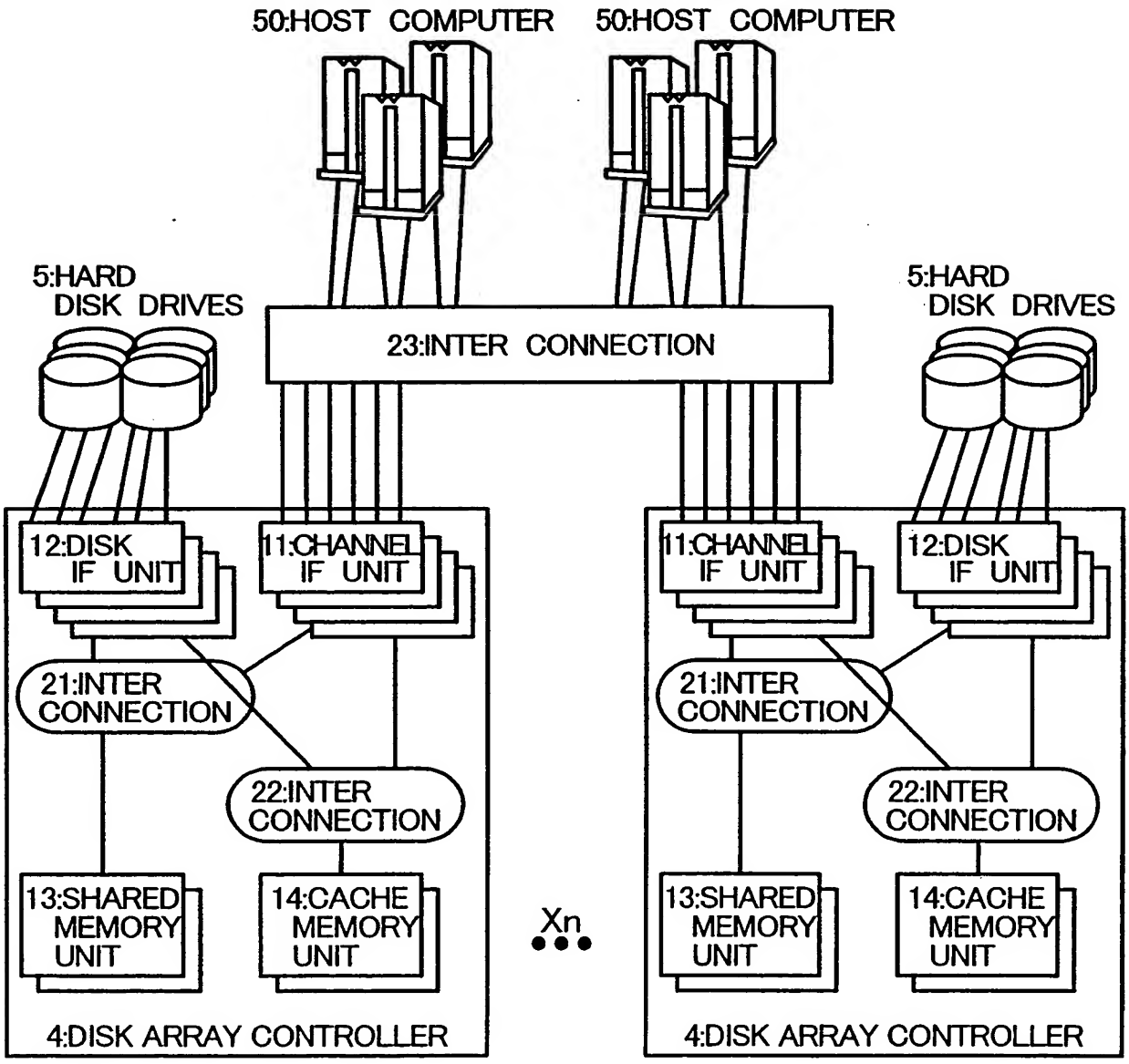

FIG.5

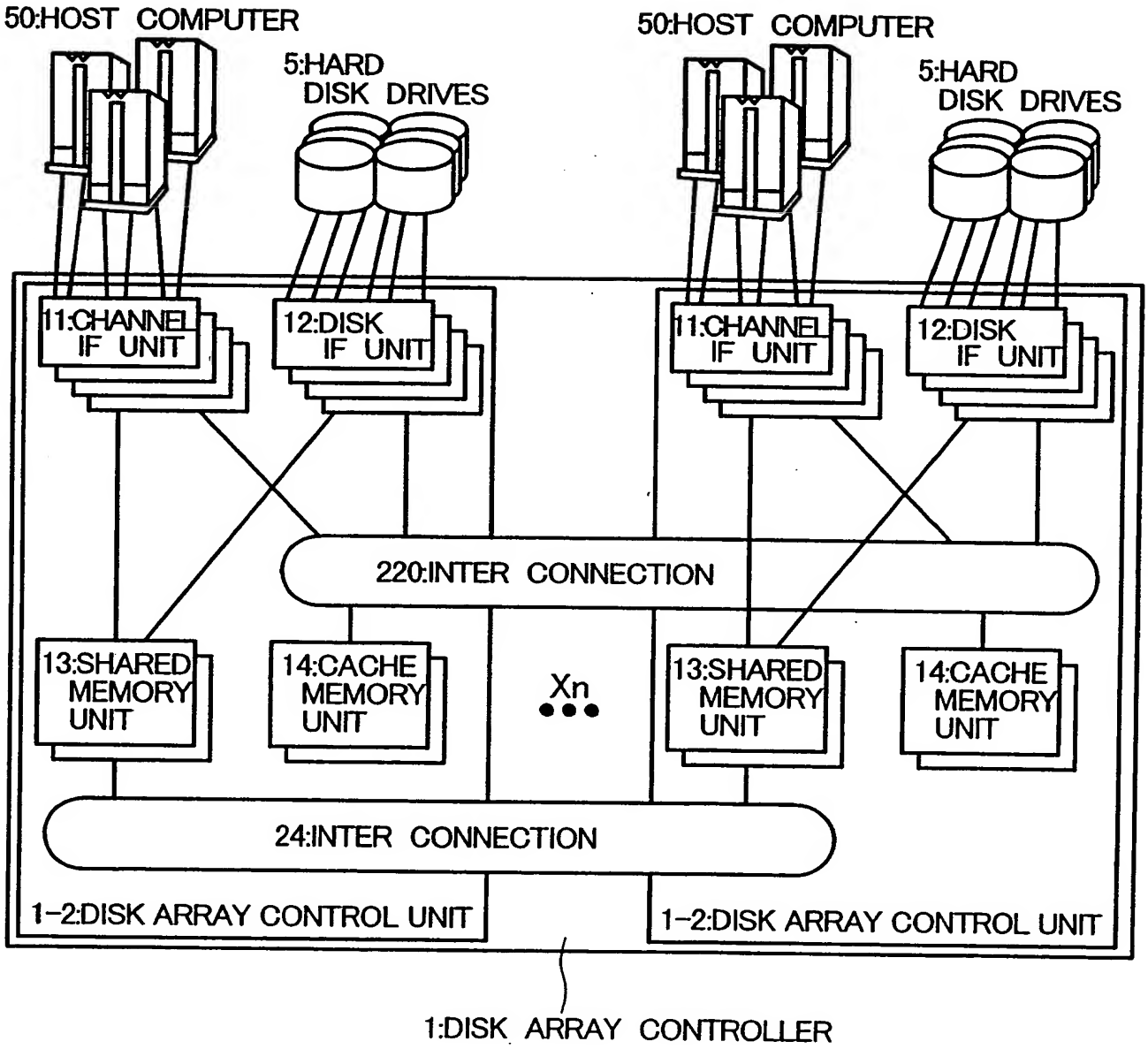
50:HOST COMPUTER
5:HARD DISK DRIVES
50:HOST COMPUTER
5:HARD DISK DRIVES
11:CHANNEL IF UNIT
12:DISK IF UNIT
11:CHANNEL IF UNIT
12:DISK IF UNIT
220:INTER CONNECTION
13:SHARED MEMORY UNIT
14:CACHE MEMORY UNIT
Xn
13:SHARED MEMORY UNIT
14:CACHE MEMORY UNIT
24:INTER CONNECTION
1-2:DISK ARRAY CONTROL UNIT
1-2:DISK ARRAY CONTROL UNIT
1:DISK ARRAY CONTROLLER

FIG.6

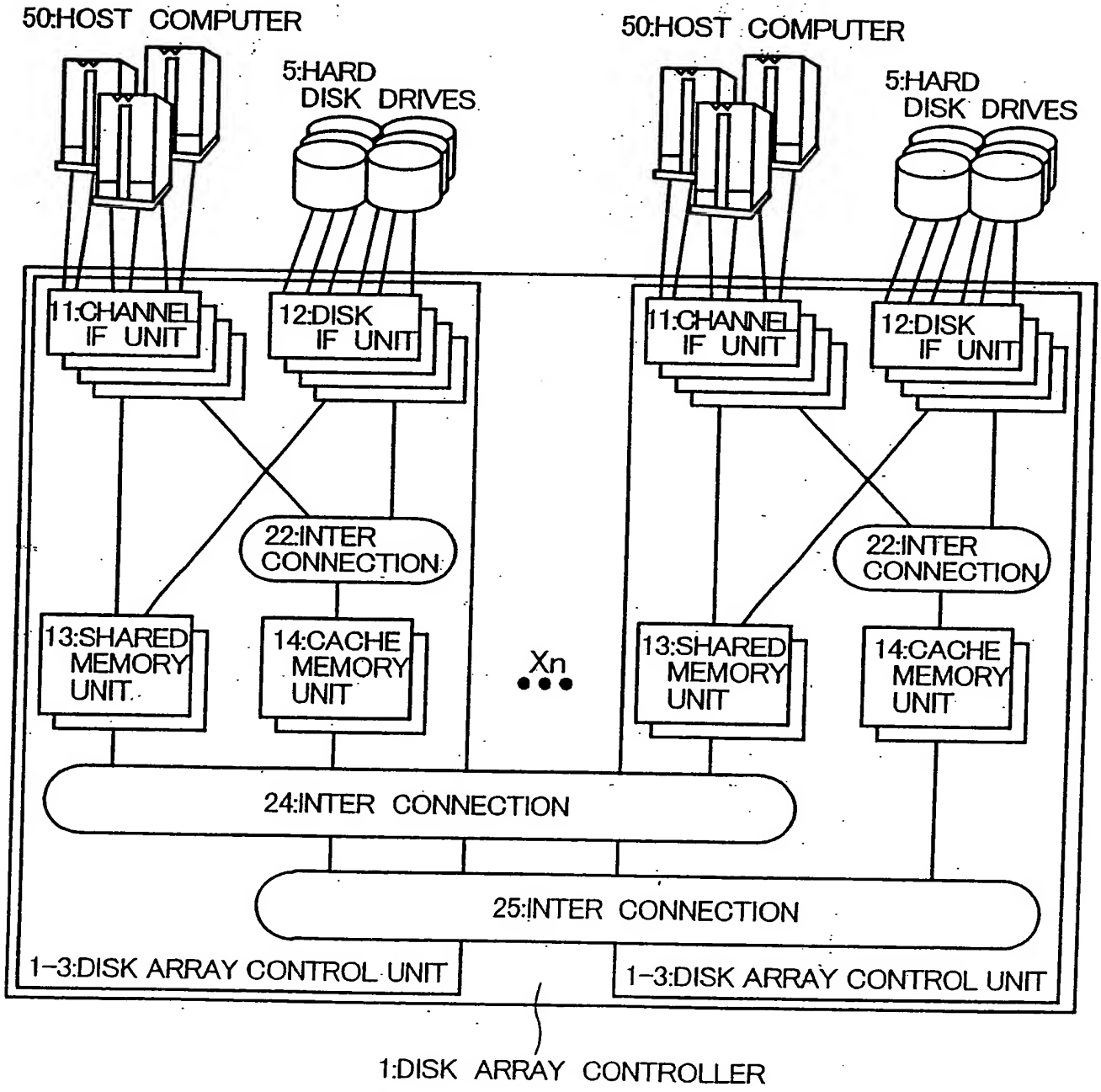
50:HOST COMPUTER
5:HARD DISK DRIVES
50:HOST COMPUTER
5:HARD DISK DRIVES
11:CHANNEL IF UNIT
12:DISK IF UNIT
11:CHANNEL IF UNIT
12:DISK IF UNIT
22:INTER CONNECTION
22:INTER CONNECTION
13:SHARED MEMORY UNIT
14:CACHE MEMORY UNIT
Xn
13:SHARED MEMORY UNIT
14:CACHE MEMORY UNIT
24:INTER CONNECTION
25:INTER CONNECTION
1-3:DISK ARRAY CONTROL UNIT
1-3:DISK ARRAY CONTROL UNIT
1:DISK ARRAY CONTROLLER

FIG.7

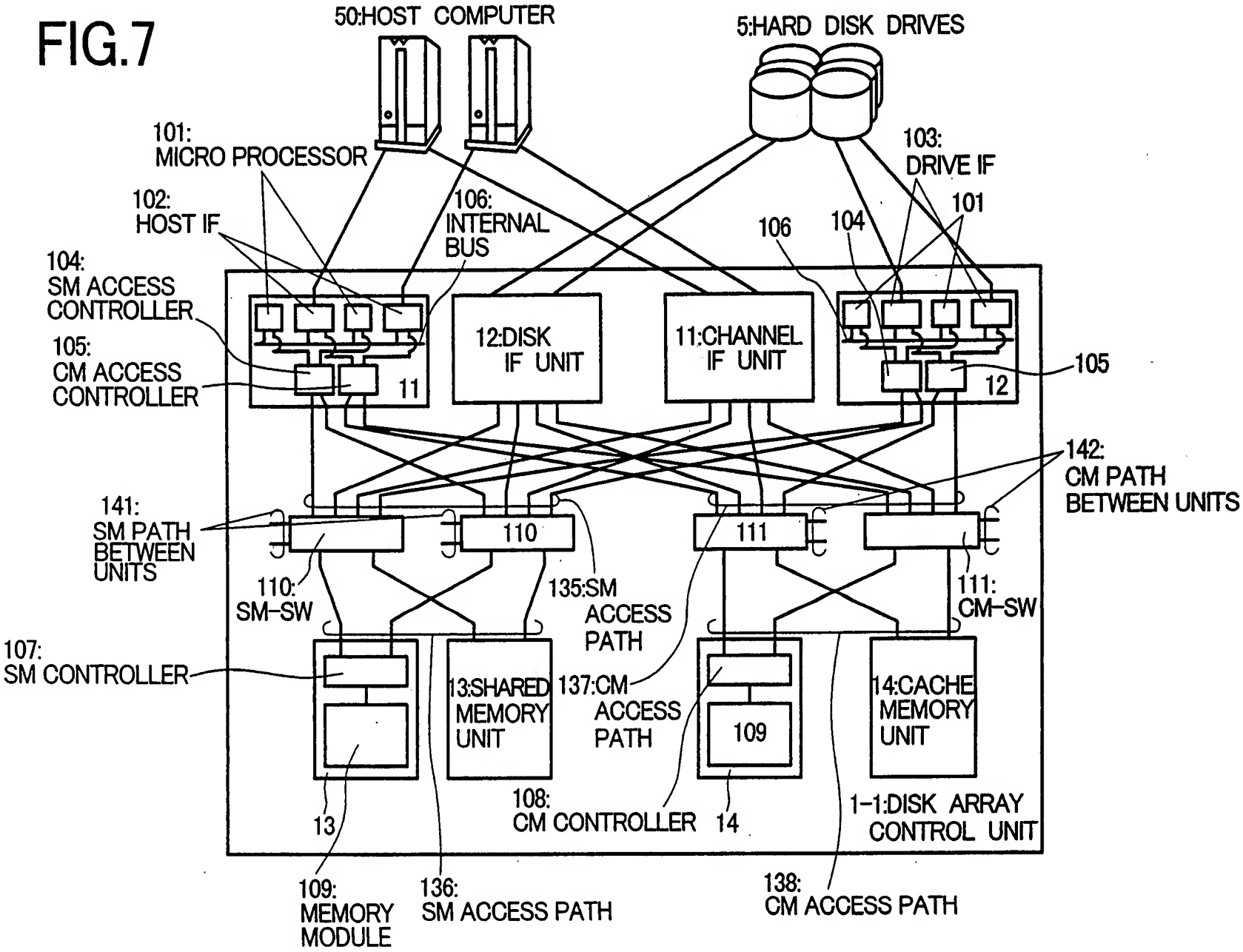
50:HOST COMPUTER
5:HARD DISK DRIVES
101:
MICRO PROCESSOR
103:
DRIVE IF
102:
HOST IF
106:
INTERNAL
BUS
101
106
104
104:
SM ACCESS
CONTROLLER
105:
CM ACCESS
CONTROLLER
11
12:DISK
IF UNIT
11:CHANNEL
IF UNIT
12
105
142:
CM PATH
BETWEEN UNITS
141:
SM PATH
BETWEEN
UNITS
110
111
110:
SM-SW
135:SM
ACCESS
PATH
111:
CM-SW
107:
SM CONTROLLER
13:SHARED
MEMORY
UNIT
137:CM
ACCESS
PATH
109
14:CACHE
MEMORY
UNIT
13
108:
CM CONTROLLER
14
1-1:DISK ARRAY
CONTROL UNIT
109:
MEMORY
MODULE
136:
SM ACCESS PATH
138:
CM ACCESS PATH

FIG.8

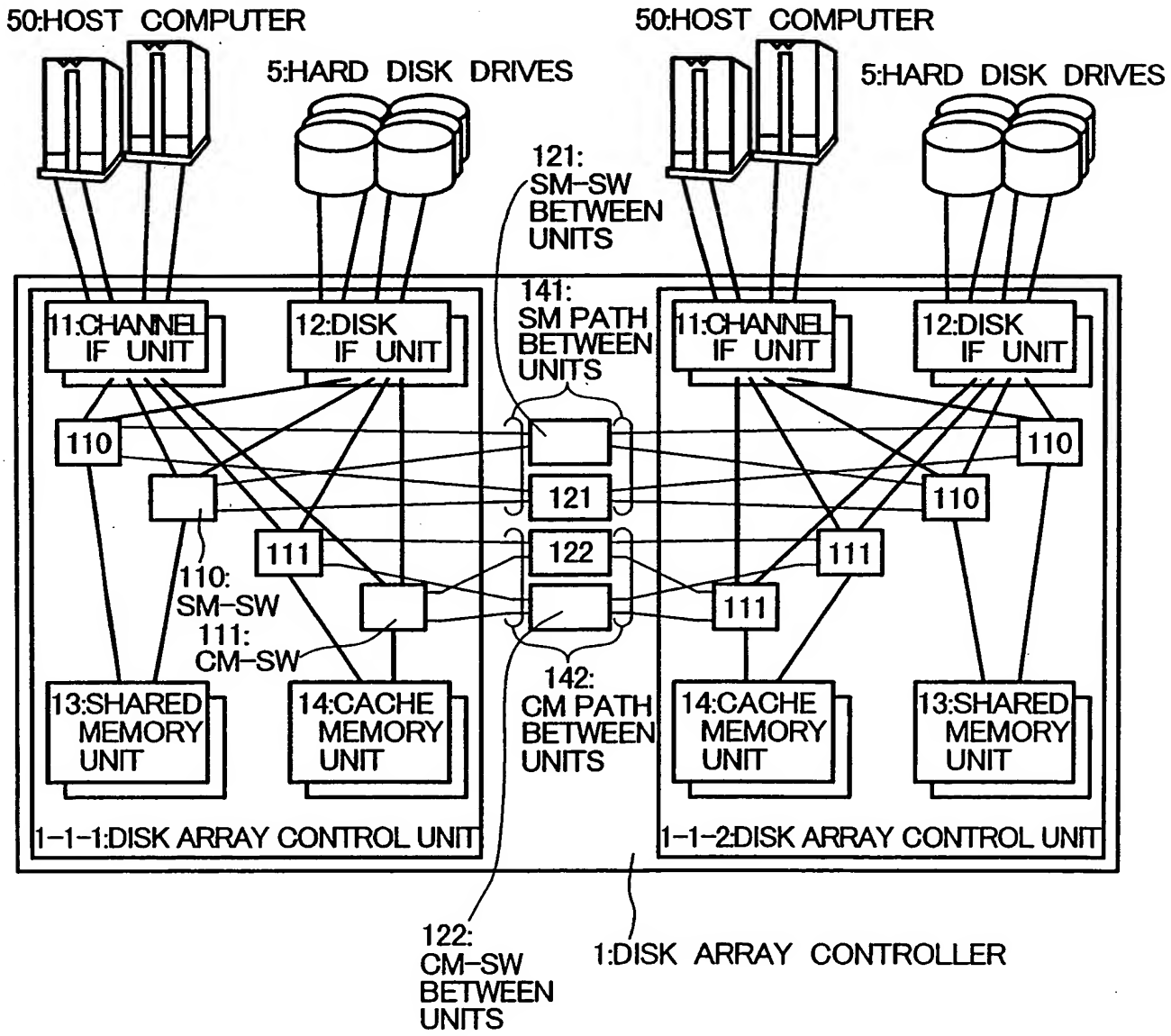
50:HOST COMPUTER
5:HARD DISK DRIVES
50:HOST COMPUTER
5:HARD DISK DRIVES
121:
SM-SW
BETWEEN
UNITS
141:
SM PATH
BETWEEN
UNITS
11:CHANNEL
IF UNIT
12:DISK
IF UNIT
11:CHANNEL
IF UNIT
12:DISK
IF UNIT
110
110
121
110
111
122
111
110:
SM-SW
111:
CM-SW
111
142:
CM PATH
BETWEEN
UNITS
13:SHARED
MEMORY
UNIT
14:CACHE
MEMORY
UNIT
14:CACHE
MEMORY
UNIT
13:SHARED
MEMORY
UNIT
1-1-1:DISK ARRAY CONTROL UNIT
1-1-2:DISK ARRAY CONTROL UNIT
122:
CM-SW
BETWEEN
UNITS
1:DISK ARRAY CONTROLLER

FIG.9

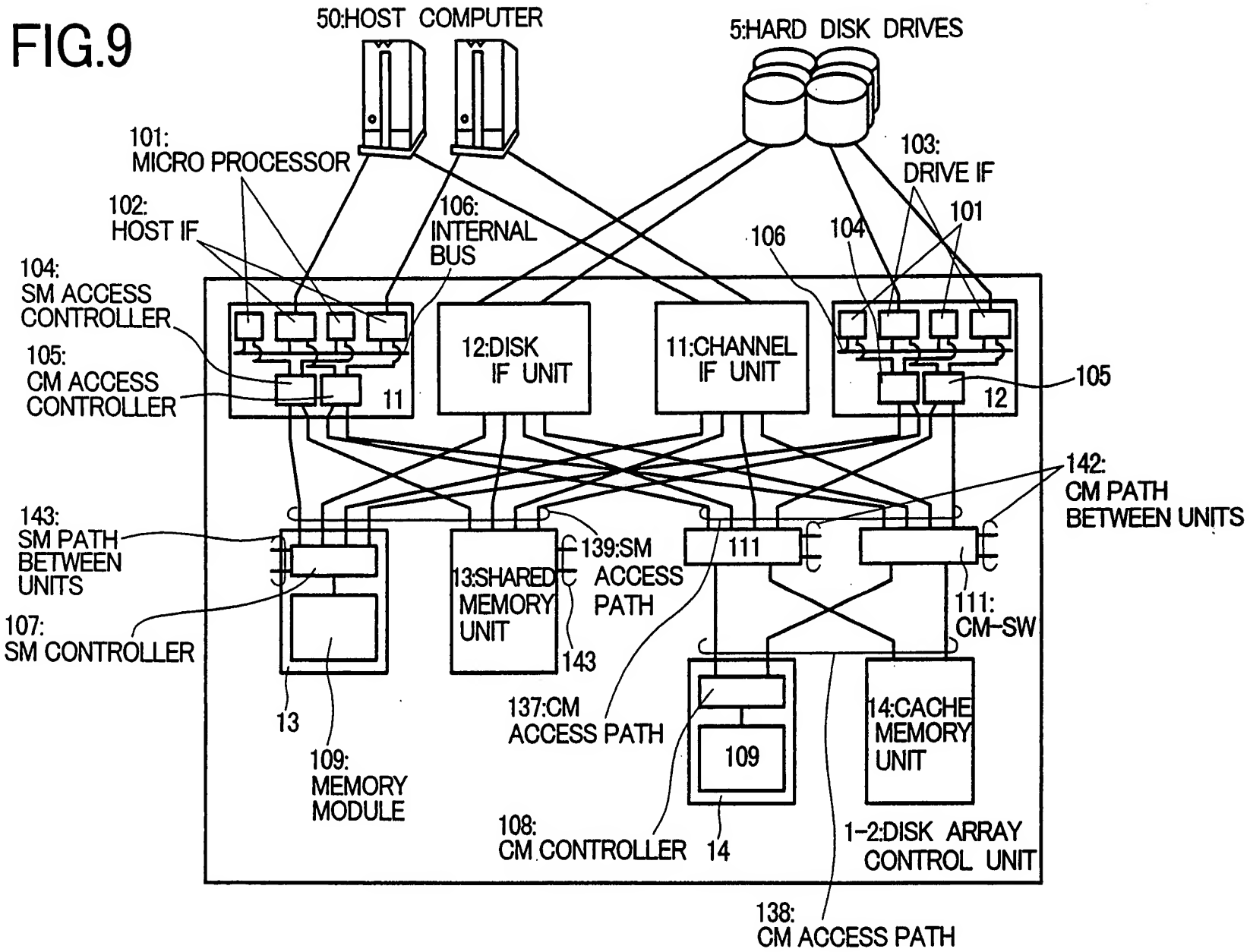
50:HOST COMPUTER
5:HARD DISK DRIVES
101:
MICRO PROCESSOR
102:
HOST IF
106:
INTERNAL
BUS
103:
DRIVE IF
101
106
104
104:
SM ACCESS
CONTROLLER
105:
CM ACCESS
CONTROLLER
12:DISK
IF UNIT
11:CHANNEL
IF UNIT
11
12
105
142:
CM PATH
BETWEEN UNITS
143:
SM PATH
BETWEEN
UNITS
107:
SM CONTROLLER
13:SHARED
MEMORY
UNIT
139:SM
ACCESS
PATH
143
111
111:
CM-SW
13
109:
MEMORY
MODULE
137:CM
ACCESS PATH
109
14:CACHE
MEMORY
UNIT
108:
CM CONTROLLER
14
1-2:DISK ARRAY
CONTROL UNIT
138:
CM ACCESS PATH

FIG.10

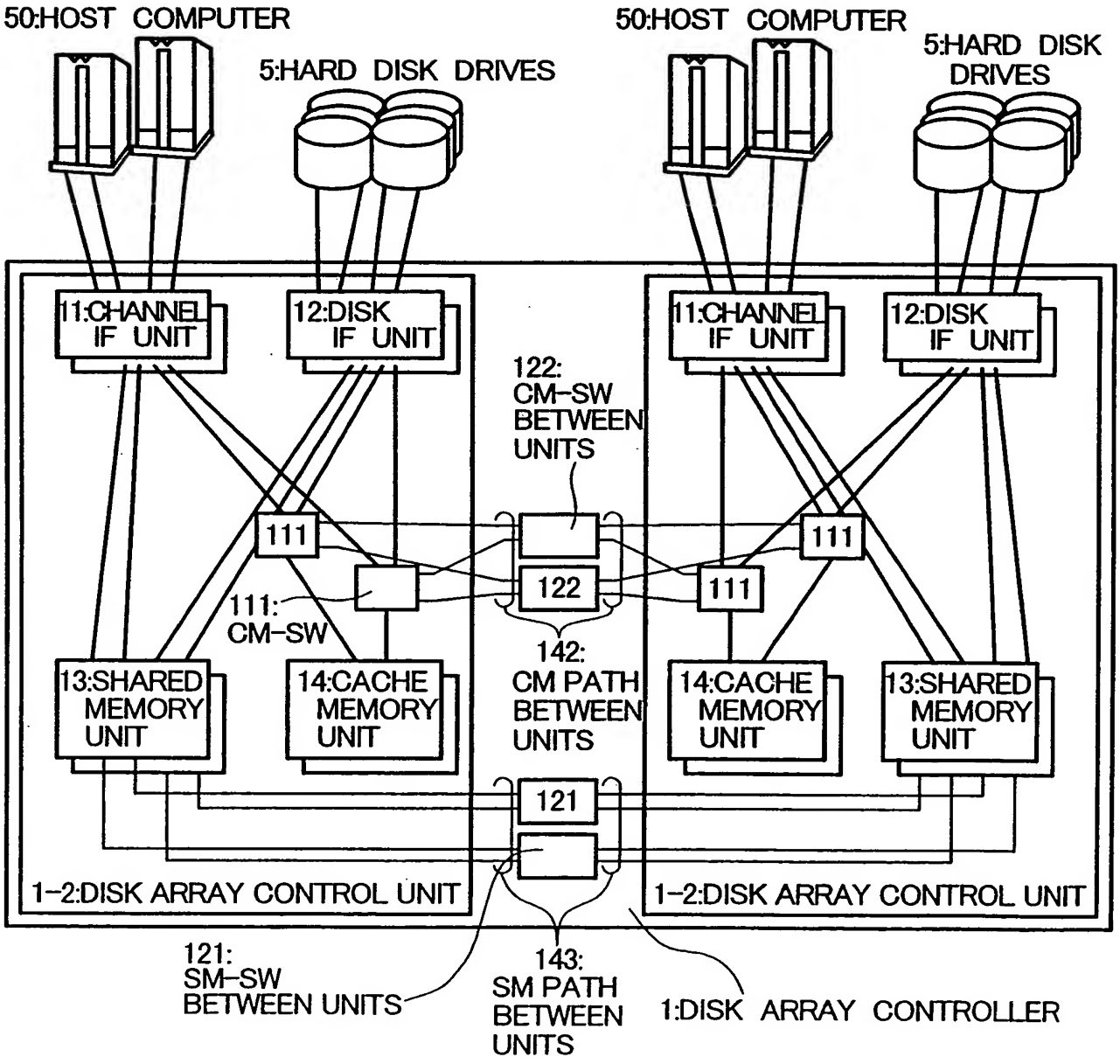
50:HOST COMPUTER
5:HARD DISK DRIVES
50:HOST COMPUTER
5:HARD DISK DRIVES
11:CHANNEL IF UNIT
12:DISK IF UNIT
11:CHANNEL IF UNIT
12:DISK IF UNIT
122: CM-SW BETWEEN UNITS
111
111
122
111
111: CM-SW
142: CM PATH BETWEEN UNITS
13:SHARED MEMORY UNIT
14:CACHE MEMORY UNIT
14:CACHE MEMORY UNIT
13:SHARED MEMORY UNIT
121
1-2:DISK ARRAY CONTROL UNIT
1-2:DISK ARRAY CONTROL UNIT
121: SM-SW BETWEEN UNITS
143: SM PATH BETWEEN UNITS
1:DISK ARRAY CONTROLLER

FIG.11

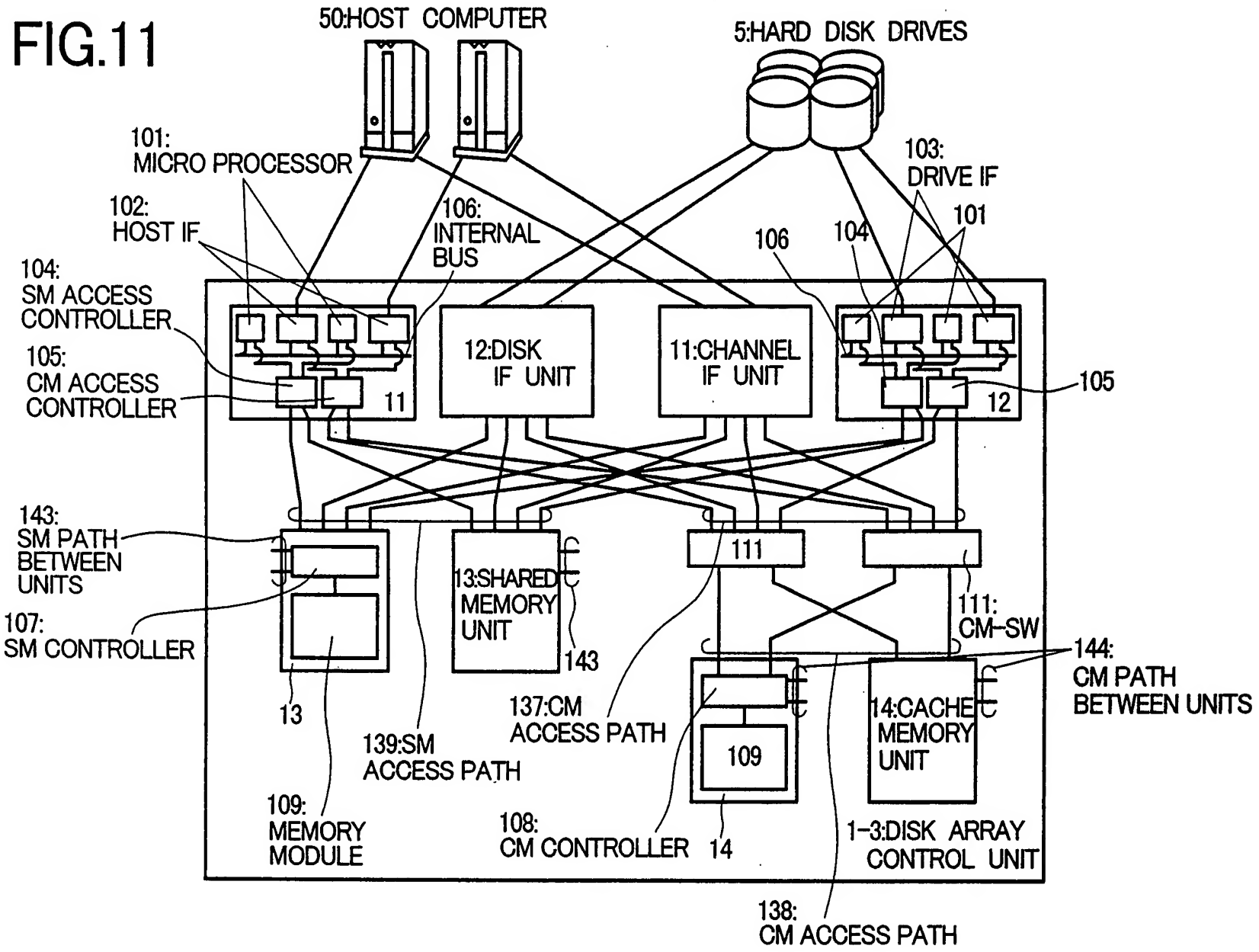
50:HOST COMPUTER
5:HARD DISK DRIVES
101:
MICRO PROCESSOR
102:
HOST IF
106:
INTERNAL
BUS
103:
DRIVE IF
101
106
104
104:
SM ACCESS
CONTROLLER
105:
CM ACCESS
CONTROLLER
12:DISK
IF UNIT
11:CHANNEL
IF UNIT
11
12
105
143:
SM PATH
BETWEEN
UNITS
107:
SM CONTROLLER
13:SHARED
MEMORY
UNIT
143
111
111:
CM-SW
144:
CM PATH
BETWEEN UNITS
13
139:SM
ACCESS PATH
137:CM
ACCESS PATH
109
14:CACHE
MEMORY
UNIT
109:
MEMORY
MODULE
108:
CM CONTROLLER
14
1-3:DISK ARRAY
CONTROL UNIT
138:
CM ACCESS PATH

FIG.12

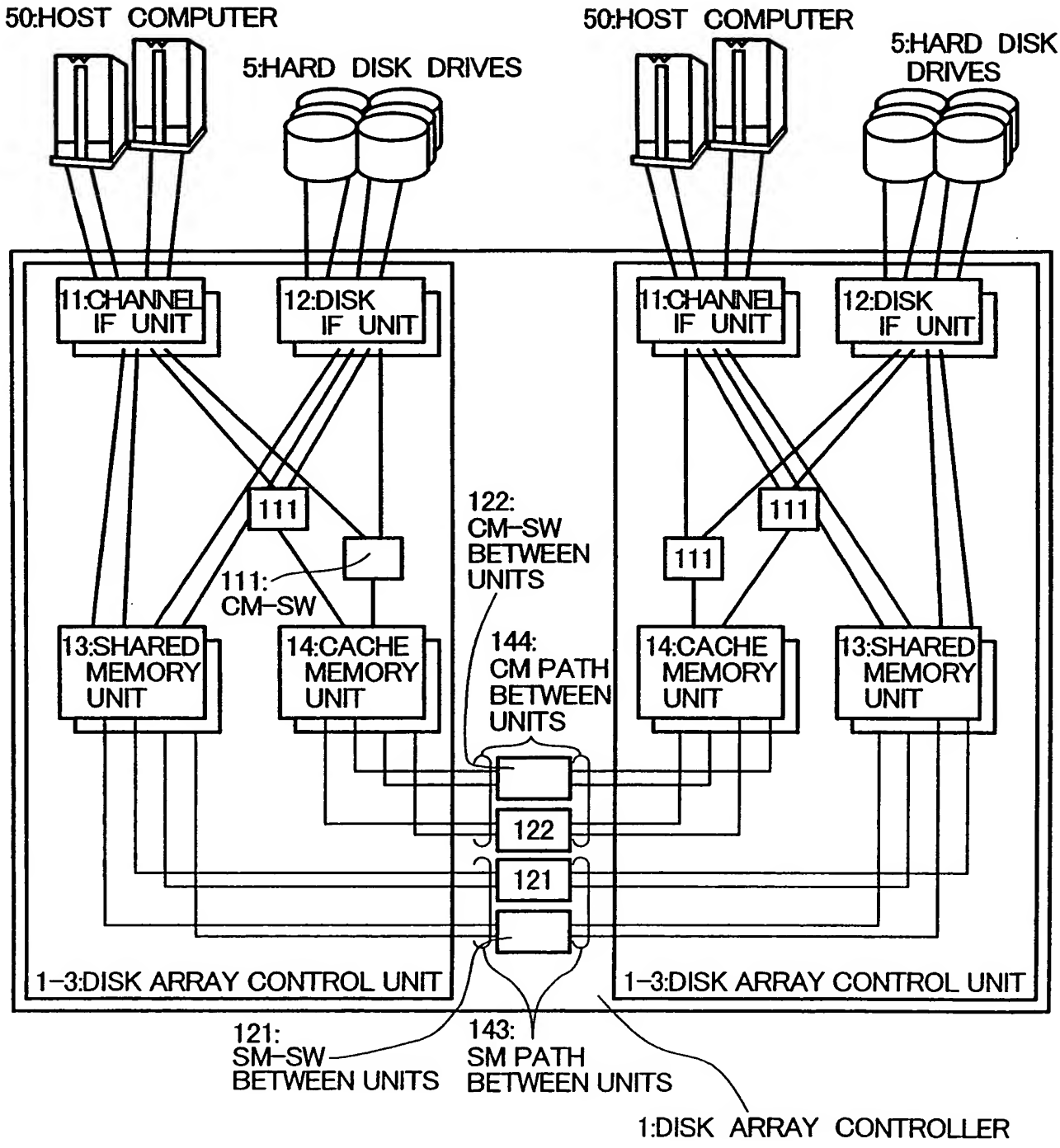
50:HOST COMPUTER
5:HARD DISK DRIVES
50:HOST COMPUTER
5:HARD DISK DRIVES
11:CHANNEL IF UNIT
12:DISK IF UNIT
11:CHANNEL IF UNIT
12:DISK IF UNIT
111
111
111
111:
CM-SW
122:
CM-SW
BETWEEN
UNITS
144:
CM PATH
BETWEEN
UNITS
13:SHARED MEMORY UNIT
14:CACHE MEMORY UNIT
14:CACHE MEMORY UNIT
13:SHARED MEMORY UNIT
122
121
1-3:DISK ARRAY CONTROL UNIT
1-3:DISK ARRAY CONTROL UNIT
121:
SM-SW
BETWEEN UNITS
143:
SM PATH
BETWEEN UNITS
1:DISK ARRAY CONTROLLER

FIG.13

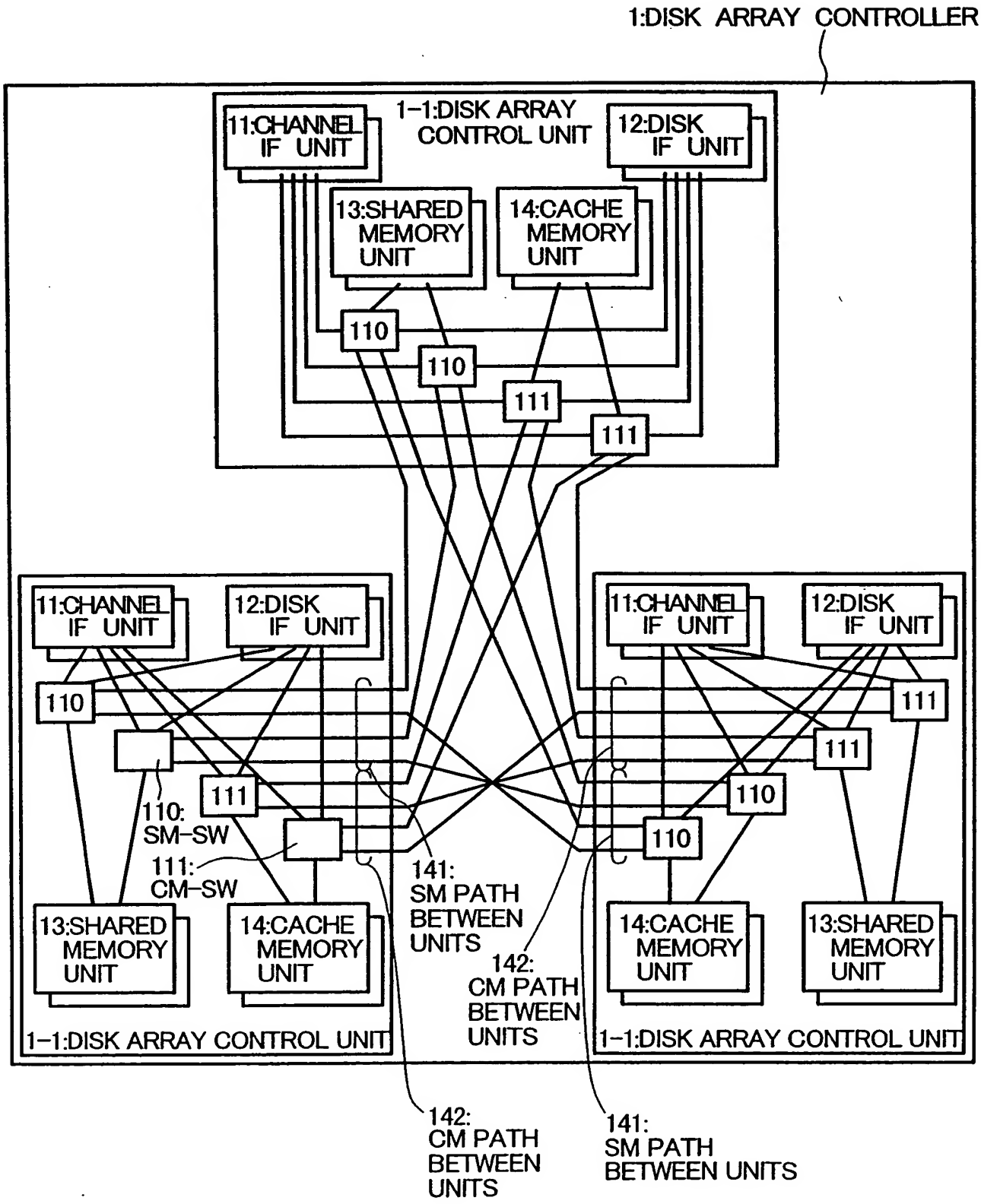
1:DISK ARRAY CONTROLLER
1-1:DISK ARRAY CONTROL UNIT
11:CHANNEL IF UNIT
12:DISK IF UNIT
13:SHARED MEMORY UNIT
14:CACHE MEMORY UNIT
110
111
110: SM-SW
111: CM-SW
141: SM PATH BETWEEN UNITS
142: CM PATH BETWEEN UNITS
1-1:DISK ARRAY CONTROL UNIT
142: CM PATH BETWEEN UNITS
141: SM PATH BETWEEN UNITS

FIG.14

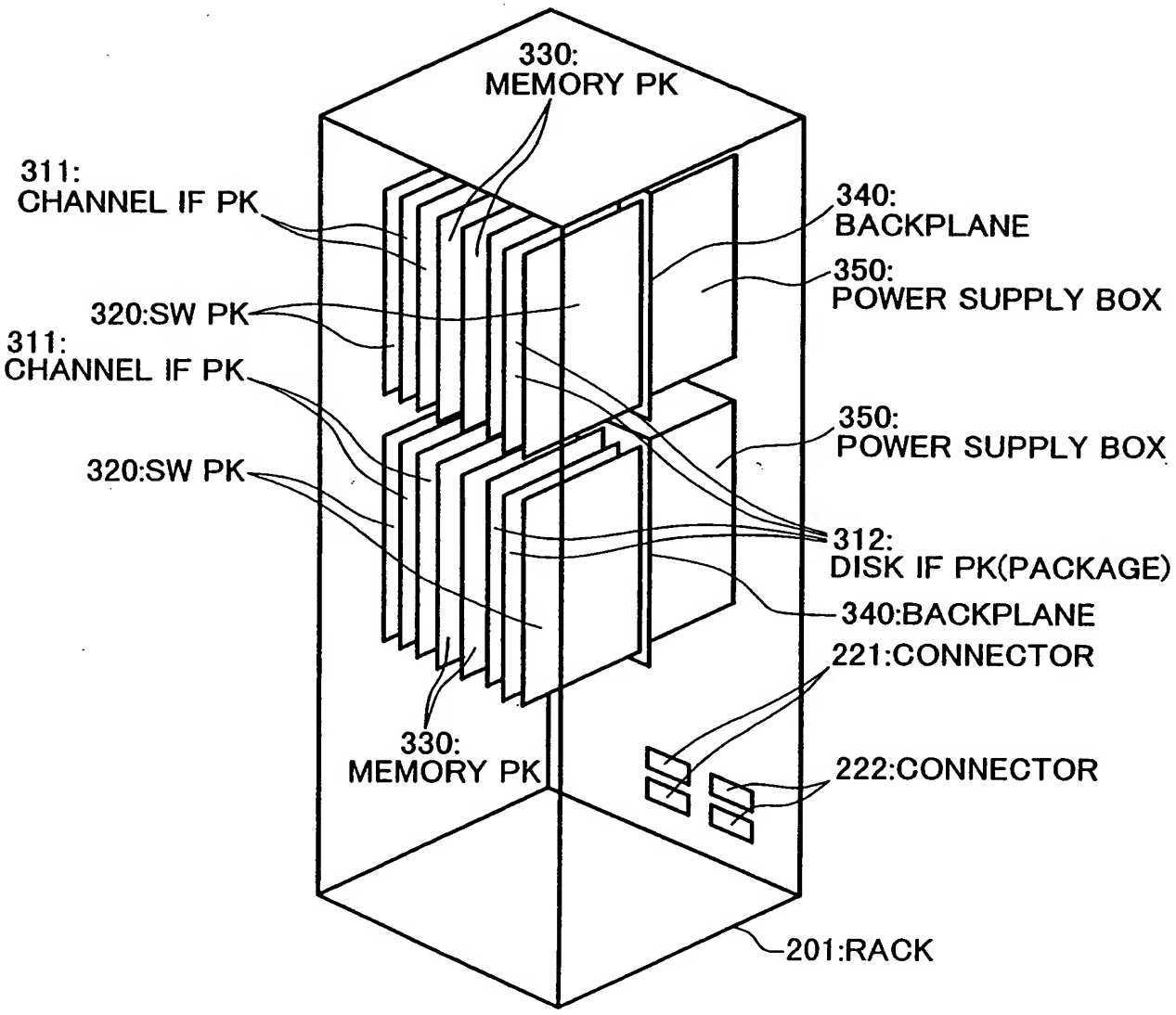
330:
MEMORY PK
311:
CHANNEL IF PK
340:
BACKPLANE
350:
POWER SUPPLY BOX
320:SW PK
311:
CHANNEL IF PK
350:
POWER SUPPLY BOX
320:SW PK
312:
DISK IF PK(PACKAGE)
340:BACKPLANE
221:CONNECTOR
330:
MEMORY PK
222:CONNECTOR
201:RACK

FIG.15

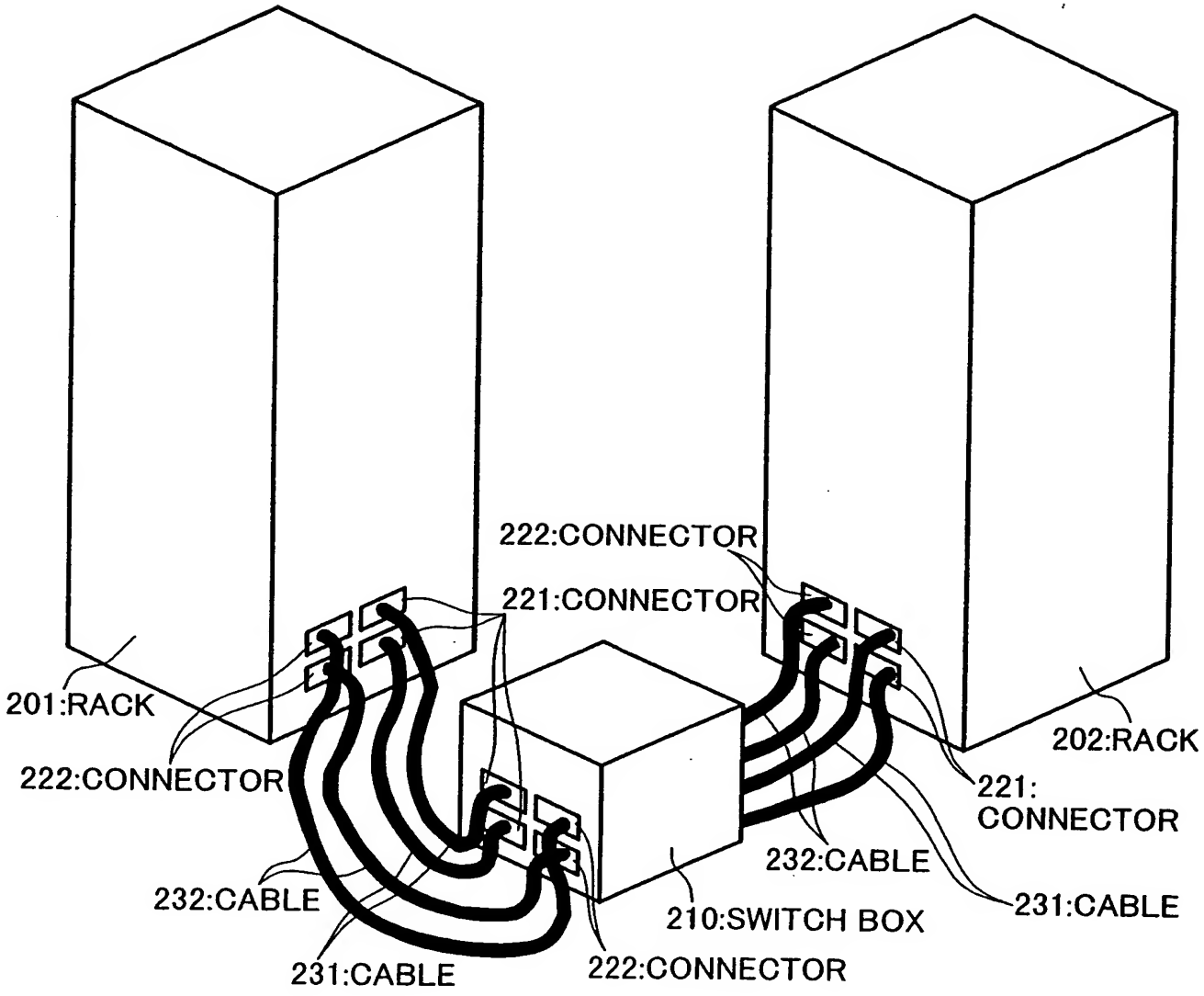
222:CONNECTOR
221:CONNECTOR
201:RACK
222:CONNECTOR
202:RACK
221:
CONNECTOR
232:CABLE
232:CABLE
231:CABLE
210:SWITCH BOX
231:CABLE
222:CONNECTOR

FIG.16

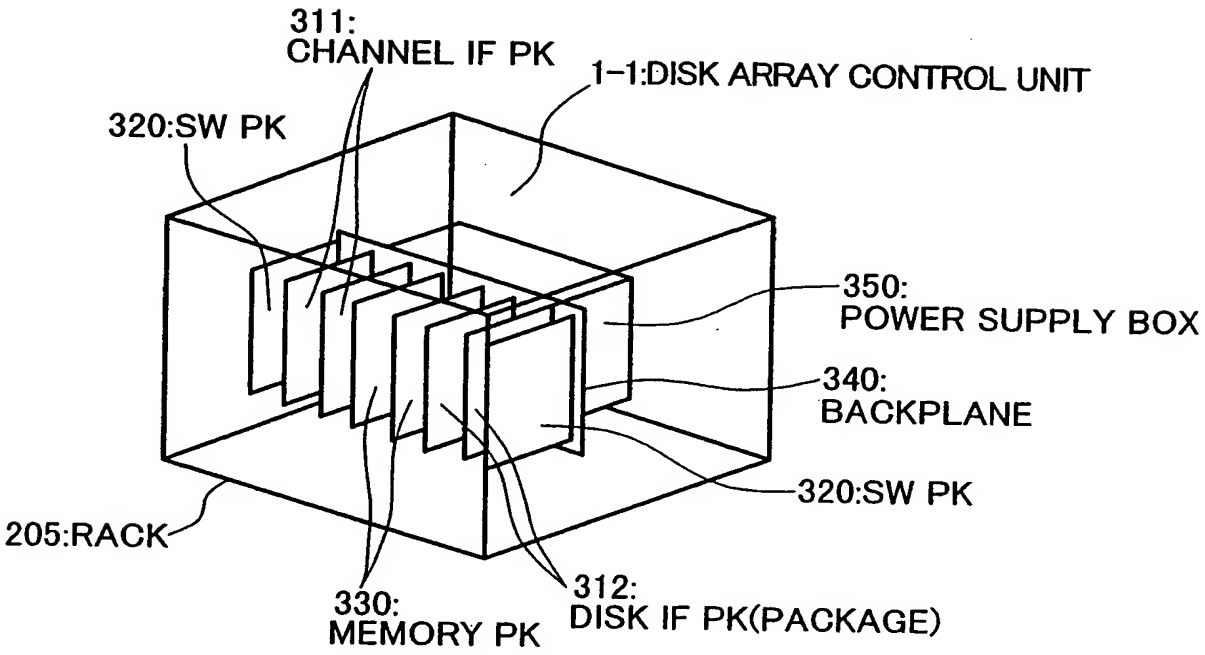
311:
CHANNEL IF PK
1-1:DISK ARRAY CONTROL UNIT
320:SW PK
350:
POWER SUPPLY BOX
340:
BACKPLANE
320:SW PK
205:RACK
330:
MEMORY PK
312:
DISK IF PK(PACKAGE)

FIG.17

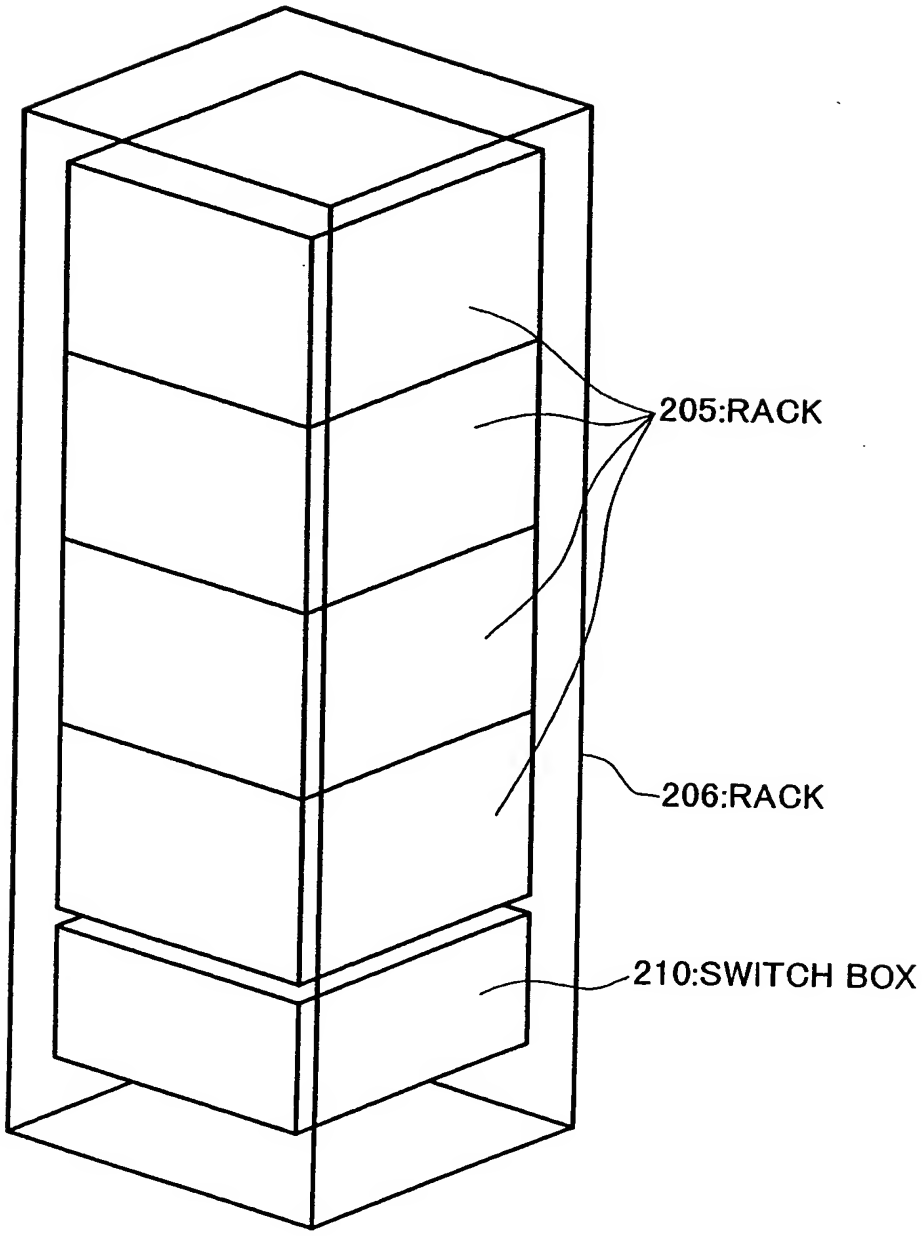

FIG.18

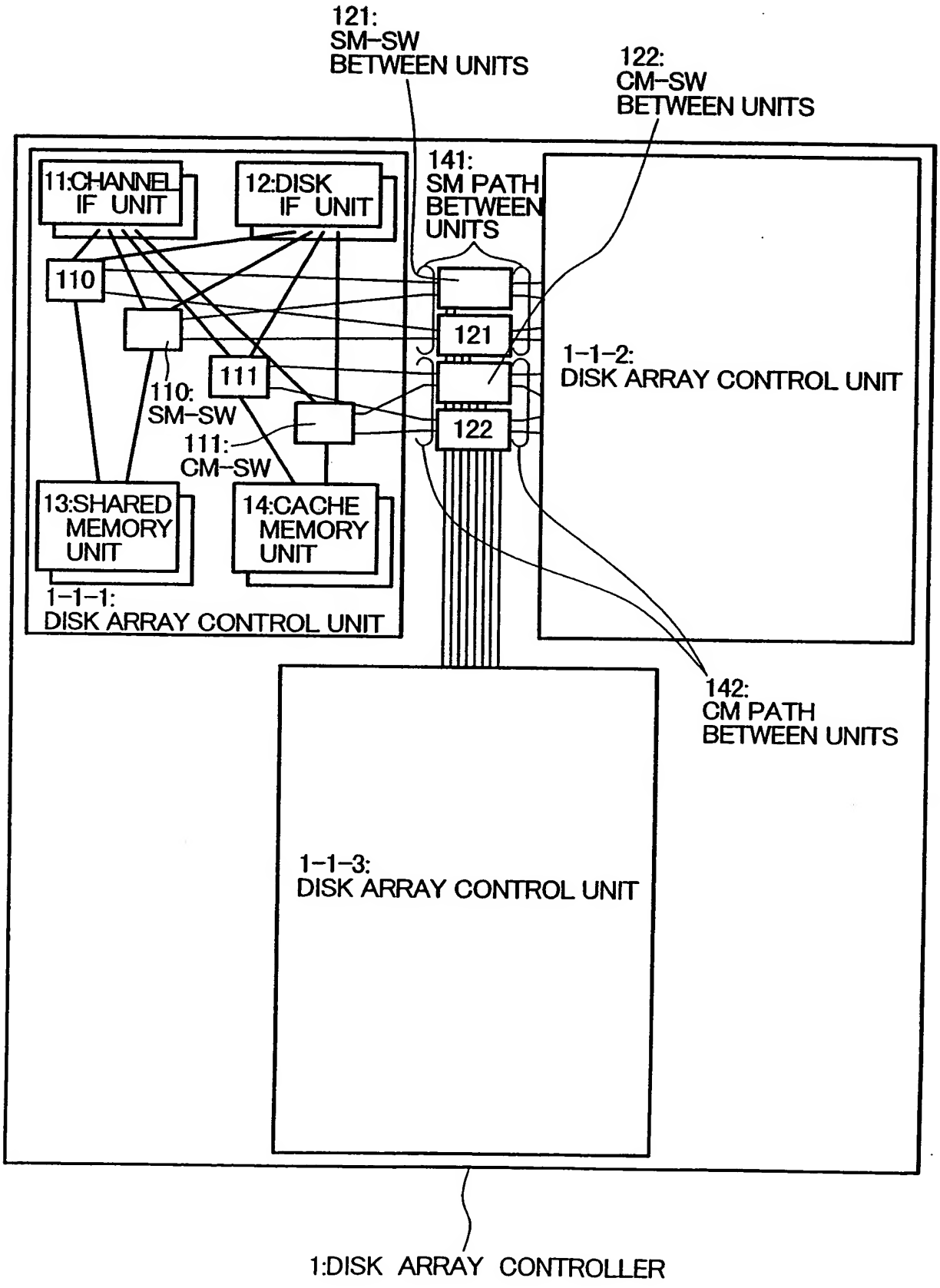
121:
SM-SW
BETWEEN UNITS
122:
CM-SW
BETWEEN UNITS
11:CHANNEL
IF UNIT
12:DISK
IF UNIT
141:
SM PATH
BETWEEN
UNITS
110
121
111
110:
SM-SW
111:
CM-SW
122
13:SHARED
MEMORY
UNIT
14:CACHE
MEMORY
UNIT
1-1-1:
DISK ARRAY CONTROL UNIT
1-1-2:
DISK ARRAY CONTROL UNIT
142:
CM PATH
BETWEEN UNITS
1-1-3:
DISK ARRAY CONTROL UNIT
1:DISK ARRAY CONTROLLER

FIG.19

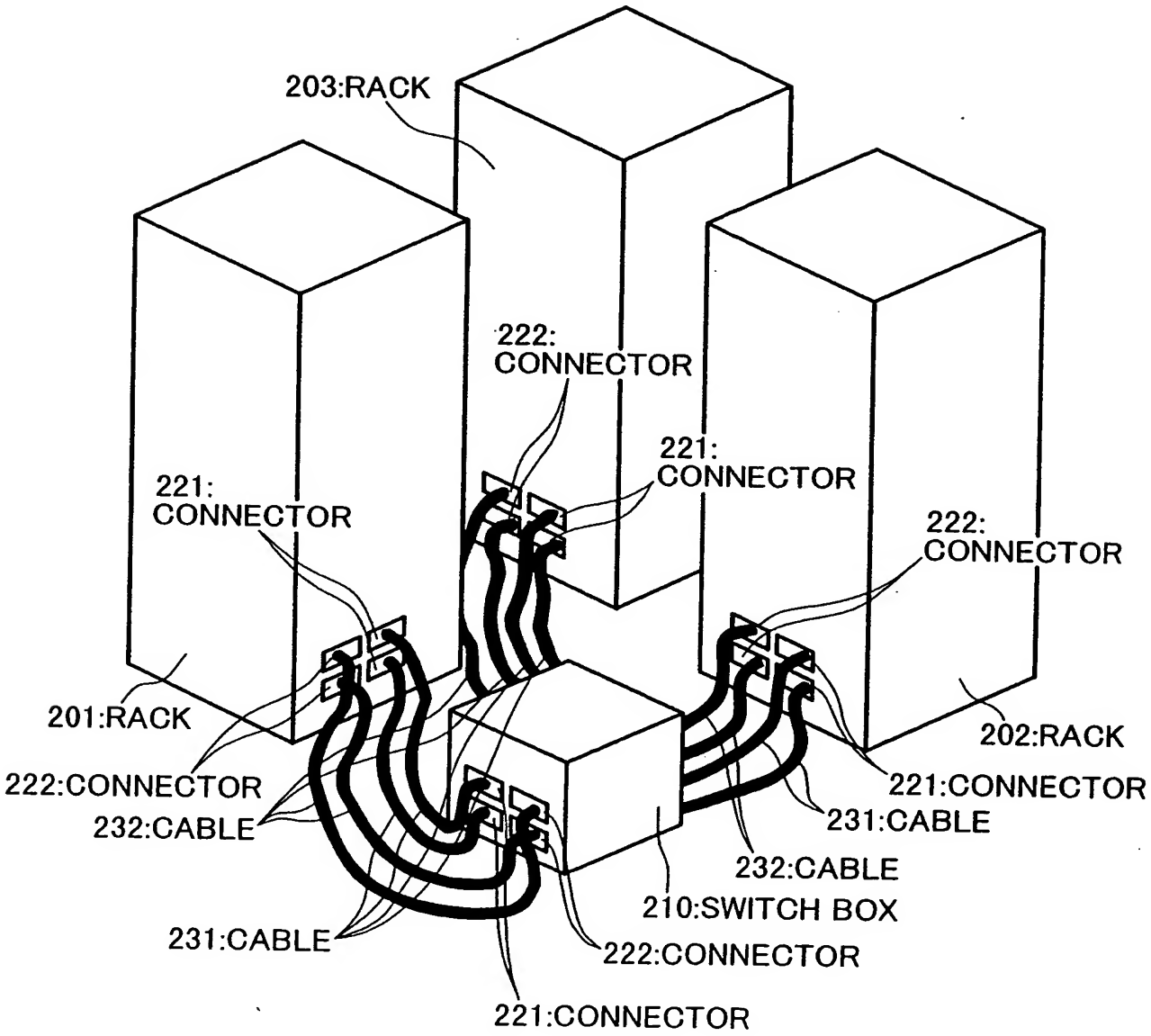
203:RACK
222:
CONNECTOR
221:
CONNECTOR
221:
CONNECTOR
222:
CONNECTOR
201:RACK
202:RACK
222:CONNECTOR
232:CABLE
221:CONNECTOR
231:CABLE
232:CABLE
210:SWITCH BOX
231:CABLE
222:CONNECTOR
221:CONNECTOR

FIG.20

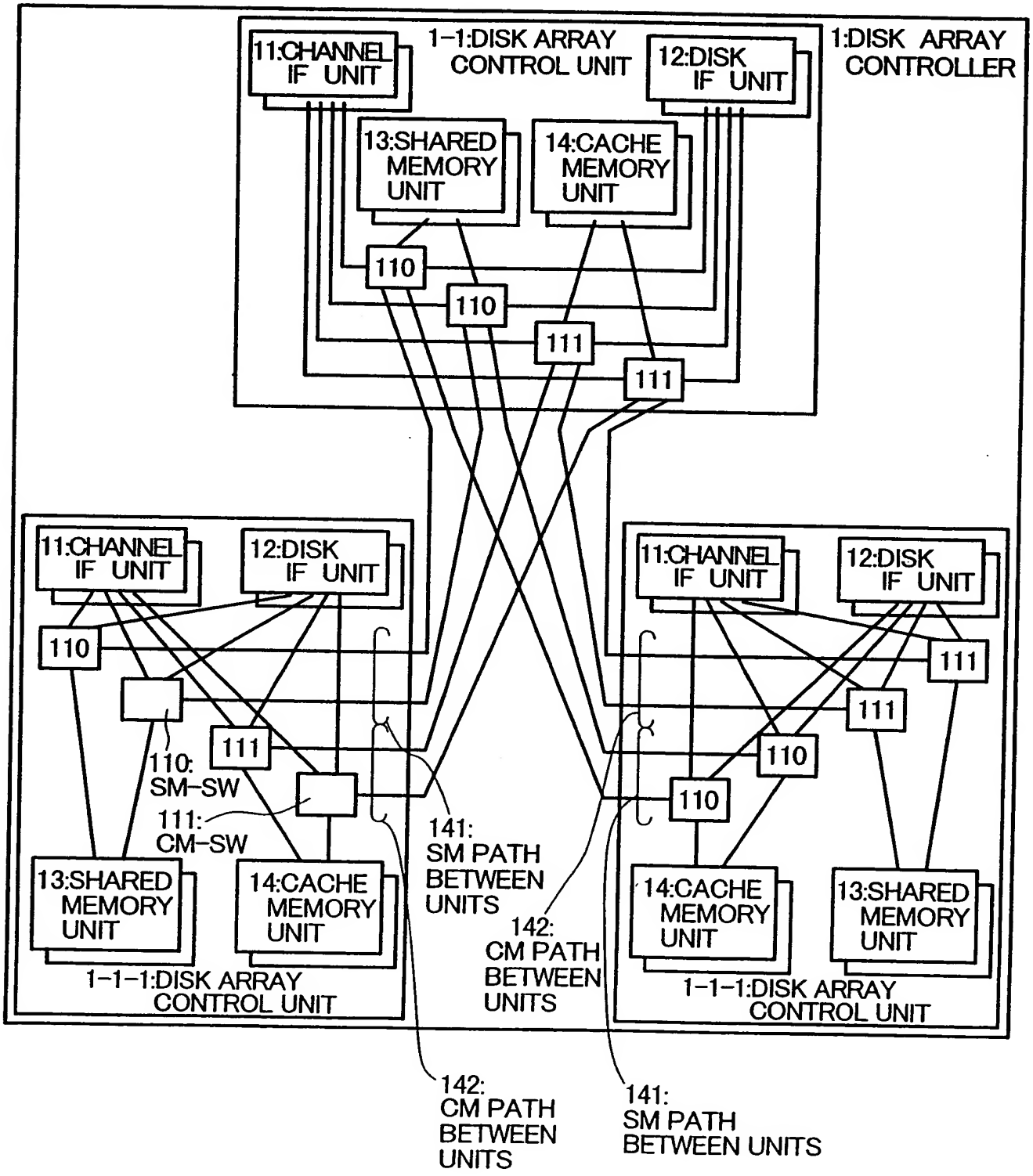
1:DISK ARRAY CONTROLLER
1-1:DISK ARRAY CONTROL UNIT
11:CHANNEL IF UNIT
12:DISK IF UNIT
13:SHARED MEMORY UNIT
14:CACHE MEMORY UNIT
110
111
1-1-1:DISK ARRAY CONTROL UNIT
110: SM-SW
111: CM-SW
141: SM PATH BETWEEN UNITS
142: CM PATH BETWEEN UNITS

FIG.21

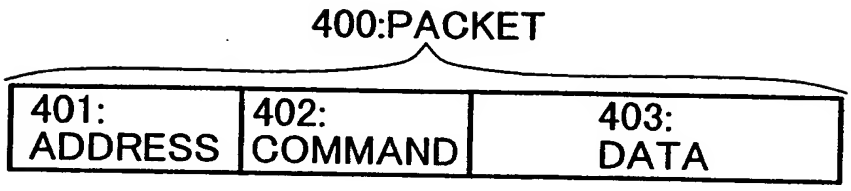

FIG.22

410:REFFERENCE TABLE
FOR PATH SWITCH

ADDRESS.	PORT No.
0×0···000	0
0×0···001	0
⋮	⋮
0×0···OFF	0
0×0···100	1
⋮	⋮
0×0···200	2
⋮	⋮